EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	25450315	@ad<"20040112"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/03 11:29
L2	29	1 and tag adj2 (buffer queue) same controller and tag near3 bus	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/03 12:12
L3	13	1 and buffer with read adj2 queue with write adj2 queue and tag	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/03 12:19
L4	48	1 and buffer with read adj2 queue with write adj2 queue	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/03 12:19
S74	830	(bidirectional bi-directional) with buffer with controller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S75	306	briggs.in.	US-PGPUB	OR	ON	2007/07/02 12:09
S76	683	711/104.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09

S77	4023	(bidirectional bi-directional) adj data adj bus	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S78	1	S75 and "tag buffer".clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S79	410	buffer with logic$2 with decod$3 with controller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S80	25449134	@ad<"20040112"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S81	263	(bidirectional bi-directional) with bus with buffer with controller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S82	18	S81 and S80 and S79	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S83	2202	711/118.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09

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S84	805	interfac$3 with buffer with read$3 with writ$3 with memory with controller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S85	7	S81 and S80 and S84	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S86	1225	711/105.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S87	2	S75 and "bidirectional".clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S88	1624	711/100.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S89	280	711/101.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S90	1323	((RAM DRAM DDRAM) with buffer) and (memory adj controller) and (control adj logic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09

S91	54	S90 and S77 and @ad<"20040112"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S92	481	711/117.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S93	3363	365/189.05.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S94	3573	365/189.01.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S95	9	(S83 S92 S86 S76 S94 S93 S88 S89) and S81 and S80	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S96	21	(S83 S92 S86 S76 S94 S93 S88 S89) and S74 and S80	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S97	116	S81 same memory and S80	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09

S98	28	S81 same memory same read$3 with writ$3 and S80	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S99	2	"20050154820".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S10 0	2	"tag buffer" same (RAM DRAM DDRAM "system memory") same control near2 signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S10 1	1	"6810475".PN.	USPAT; USOCR	OR	ON	2007/07/02 12:09
S10 2	1	"20030005263".PN.	US-PGPUB	OR	ON	2007/07/02 12:09
S10 3	1	"20030158992".PN.	US-PGPUB	OR	ON	2007/07/02 12:09
S10 4	1	"4683555".PN.	USPAT; USOCR	OR	ON	2007/07/02 12:09
S10 5	25449134	@ad<"20040112"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S10 6	1	S105 and S100	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S10 7	48	read near2 (queue pipeline buffer) same write near2 (queue pipeline buffer) same tag near2 (queue pipeline buffer) and S105	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09

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S10 8	1	"6754772".PN.	USPAT; USOCR	OR	ON	2007/07/02 12:09
S10 9	4	(RAM DRAM DDRAM "system memory") same tag near2 (buffer queue) same control with signal same controller and S105	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S11 0	25	(RAM DRAM DDRAM) same tag adj (buffer queue) same controller and S105	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S11 1	9	(RAM DRAM DDRAM "system memory") same tag near2 (buffer queue) same control with signal and S105	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S11 2	21	(RAM DRAM DDRAM) same "tag buffer" same controller and S105	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S11 3	1	read near2 queue same write near2 queue same buffer same tag near2 queue and S105	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S11 4	4	(RAM DRAM DDRAM "system memory") same "read queue" same "write queue" same buffer and S105	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S11 5	10	(RAM DRAM DDRAM "system memory") same "read queue" same "write queue" same tag and S105	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09

S11 6	45	(RAM DRAM DDRAM "system memory") same tag near2 (buffer queue) same controller and S105	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S11 7	2	"read queue" same "write queue" same buffer with tag and S105	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S11 8	8	(RAM DRAM DDRAM "system memory") same tag near2 (buffer queue) same read$3 same writ$3 and control with signal same (controller "control logic") and S105	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S11 9	65	(RAM DRAM DDRAM "system memory") same tag near2 (buffer queue) and control with signal same (controller "control logic") and S105	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S12 0	95	(RAM DRAM DDRAM) same buffer with tag same controller and S105	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S12 1	1044	(RAM DRAM DDRAM "system memory") same read near2 (buffer queue) same write near2 (buffer queue) and S105	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09
S12 2	1	"6400684".PN.	USPAT; USOCR	OR	ON	2007/07/02 12:09
S12 3	1323	((RAM DRAM DDRAM) with buffer) and (memory adj controller) and (control adj logic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 12:09

S12 4	2	"4796232".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 19:29
S12 5	2	"6363444".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 17:27
S12 6	2	"6546464".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 17:27
S13 0	25449134	@ad<"20040112"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 18:00
S13 1	1727958	(buffer cache register)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 18:01
S13 2	893037	(bus$2 BIU)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 18:01
S13 3	1655346	controller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 18:01

S13 4	40526	S130 and S131 same S132 same S133	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 18:02
S13 5	20539	S130 and S131 with S132 with S133	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 18:03
S13 6	964529	buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 18:03
S13 7	344025	read$3 near2 writ$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 18:04
S13 8	11937512	(between interpos$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 18:04
S13 9	9803	S130 and S136 with S132 with S133	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 18:08
S14 0	200	S130 and S136 with S132 with S133 with S138 same S137	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 18:06

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S14 1	2202	711/118.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 18:08
S14 2	2	S140 and S141	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 18:08
S14 3	118	S139 and S141	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 18:33
S14 4	737414	(RAM (random adj access adj memory))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 18:26
S14 5	473	S130 and S131 with S132 with S133 same S137 same S144	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 18:24
S14 6	98	S130 and S131 with S132 with S133 with S138 same S137 same S144	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 18:25
S14 7	9154	S144 near2 S132	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 18:26

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S14 8	31	S130 and S131 near5 S133 same S137 same S147	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 18:28
S14 9	772549	((system adj memor$3) RAM (random adj access adj memor$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 18:33
S15 0	557	S130 and (buffer cache) with S138 with S149 same S137	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 18:34
S15 1	22	S150 and S141	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 18:37
S15 2	6	S130 and (buffer cache) with BIU with bus with ((system adj memory) RAM) with controller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 18:38
S15 3	15	S130 and (buffer cache) with ((system adj memory) RAM) with controller same BIU	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 18:40
S15 4	15468	S130 and (buffer cache) with controller with (BIU bus$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 18:40

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S15 5	6605	S130 and (buffer cache) near5 controller near5 (BIU bus$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 18:41
S15 6	221	S155 and S141	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 18:47
S15 7	137	S130 and system near3 bus near3 buffer same S137	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 18:50
S15 8	3	S157 and S141	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 18:50
S15 9	2	("2001/0052060").URPN.	USPAT	OR	ON	2007/07/02 18:51
S16 0	1	S130 and S159	USPAT	OR	ON	2007/07/02 19:02
S16 1	508	"tag buffer"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 20:08
S16 2	0	S130 and S161 with controller with (RAM (system adj memory)) and tag near3 interface near3 control near3 bus	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 20:09

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S16 3	0	S130 and S161 with controller with (RAM (system adj memory)) and tag near3 interface near3 control	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 20:10
S16 4	7	S130 and tag adj2 (buffer cache) with controller with (RAM (system adj memory)) and tag near3 interface	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 20:12
S16 5	0	S130 and S161 with controller same (RAM (system adj memory)) and tag near3 interface	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 20:13
S16 6	1	S130 and S161 same controller same (RAM (system adj memory)) and tag near3 interface	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 20:17
S16 7	49	S130 and tag adj2 (buffer cache queue) same controller same (RAM (system adj memory)) and tag near3 interface	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 20:21
S16 8	34	S130 and tag adj2 (buffer cache queue) with controller and tag near3 interface	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 20:24
S16 9	14	S130 and tag near2 (buffer queue) with controller and tag near3 interface	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 20:24

S17 0	2	S130 and tag adj2 (buffer queue) same controller same bus$3 same (memory RAM) and tag near3 interface	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 20:25
S17 1	4	S130 and tag adj2 (buffer queue) same controller same bus$3 and tag near3 interfac$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/02 20:26
S17 2	17	S130 and tag adj2 (buffer queue) same controller and tag near3 interfac$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/03 11:29

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        <and> (read queue<in>metadata)

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        <and> (read queue<in>metadata)

#3   ((controller<in>metadata) <and> (buffer<in>metadata))

#4   ((controller<in>metadata) <and> (buffer<in>metadata))
        <and> (queue<in>metadata)

#5   ((buffer<in>metadata) <and> (read queue<in>metadata))
        <and> (write queue<in>metadata)

#6   ((tag buffer<in>metadata) <and> (controller<in>metadata))
        <and> (system bus<in>metadata)

#7   ((tag buffer<in>metadata) <and> (controller<in>metadata))
        <and> (system bus<in>metadata)

#8   ((interface<in>metadata) <and> (controller<in>metadata))
        <and> (buffer<in>metadata)

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1 Tempest and typhoon: user-level shared memory   ⬛
◆ S. K. Reinhardt, J. R. Larus, D. A. Wood
   April 1994 **ACM SIGARCH Computer Architecture News , Proceedings of the 21ST annual international symposium on Computer architecture ISCA '94**, Volume 22 Issue 2
   Publisher: IEEE Computer Society Press, ACM Press

   Full text available: 📄.pdf(1.44 MB)   Additional Information: full citation, abstract, references, citings, index terms

   Future parallel computers must efficiently execute not only hand-coded applications but also programs written in high-level, parallel programming languages. Today's machines limit these programs to a single communication paradigm, either message-passing or shared-memory, which results in uneven performance. This paper addresses this problem by defining an interface, *Tempest*, that exposes low-level communication and memory-system mechanisms so programmers and compilers can customize polici ...

2 Tempest and typhoon: user-level shared memory   ⬛
◆ Steven K. Reinhardt, James R. Larus, David A. Wood
   August 1998 **25 years of the international symposia on Computer architecture (selected papers) ISCA '98**
   Publisher: ACM Press
   Full text available: 📄.pdf(1.57 MB)   Additional Information: full citation, references, index terms

3 Cache Memories   ⬛
◆ Alan Jay Smith
   September 1982 **ACM Computing Surveys (CSUR)**, Volume 14 Issue 3
   Publisher: ACM Press
   Full text available: 📄.pdf(4.61 MB)   Additional Information: full citation, references, citings, index terms

4 Reliability and security: Hardware assisted control flow obfuscation for embedded   ⬛
◆ processors
   Xiaotong Zhuang, Tao Zhang, Hsien-Hsin S. Lee, Santosh Pande
   September 2004 **Proceedings of the 2004 international conference on Compilers,**

architecture, and synthesis for embedded systems CASES '04
Publisher: ACM Press

Full text available: 📄 pdf(275.14 KB)   Additional Information: full citation, abstract, references, citings, index terms

With more applications being deployed on embedded platforms, software protection becomes increasingly important. This problem is crucial on embedded systems like financial transaction terminals, pay-TV access-control decoders, where adversaries may easily gain full physical accesses to the systems and critical algorithms must be protected from being cracked. However, as this paper points out that protecting software with either encryption or obfuscation cannot completely preclude the control flo ...

Keywords: control flow graph, obfuscation

5   Cache memory performance in a unix enviroment
Cedell Alexander, William Keshlear, Furrokh Cooper, Faye Briggs
June 1986 **ACM SIGARCH Computer Architecture News**, Volume 14 Issue 3
Publisher: ACM Press
Full text available: 📄 pdf(2.10 MB)   Additional Information: full citation, citings, index terms

6   A memory management unit and cache controller for the MARS system
Feipei Lai, Chyuan-Yow Wu, Tai-Ming Parng
November 1990 **Proceedings of the 23rd annual workshop and symposium on Microprogramming and microarchitecture MICRO 23**
Publisher: IEEE Computer Society Press
Full text available: 📄 pdf(1.07 MB)   Additional Information: full citation, abstract, references

For large caches, the interaction between cache access and address translation affects the machine cycle time and the access time to memory. The physically addressed caches slow down the cache access due to the virtual address translation. The virtually addressed caches is faster, but the synonym problem is difficult to handle. By some software constraints and hardware support, our virtually addressed physically tagged caches can achieve the same speed as traditional virtually addressed cac ...

7   A survey of commercial parallel processors
Edward Gehringer, Janne Abullarade, Michael H. Gulyn
September 1988 **ACM SIGARCH Computer Architecture News**, Volume 16 Issue 4
Publisher: ACM Press
Full text available: 📄 pdf(2.96 MB)   Additional Information: full citation, abstract, citings, index terms

This paper compares eight commercial parallel processors along several dimensions. The processors include four shared-bus multiprocessors (the Encore Multimax, the Sequent Balance system, the Alliant FX series, and the ELXSI System 6400) and four network multiprocessors (the BBN Butterfly, the NCUBE, the Intel iPSC/2, and the FPS T Series). The paper contrasts the computers from the standpoint of interconnection structures, memory configurations, and interprocessor communication. Also, the share ...

8   Architectural Support for High Speed Protection of Memory Integrity and Confidentiality in Multiprocessor Systems
Weidong Shi, Hsien-Hsin S. Lee, Mrinmoy Ghosh, Chenghuai Lu
September 2004 **Proceedings of the 13th International Conference on Parallel Architectures and Compilation Techniques PACT '04**
Publisher: IEEE Computer Society
Full text available: Additional Information:

.pdf(255.33 KB)   full citation, abstract

Recently there is a growing effort in both the architecture and the security community to create a hardware solution for authenticating system memory.As shown in the previous work, hardware-based memory authentication will become a vital component for creating future trusted computing environments and digital rights protection.Almost all these prior work have focused on authenticating memory exclusively owned by a single processing element.However, in today's computing platforms, memory is often ...

9   Design and Implementation of High-Performance Memory Systems for Future Packet
    Buffers
Jorge García, Jesús Corbal, Llorenç Cerdà, Mateo Valero
December 2003 **Proceedings of the 36th annual IEEE/ACM International Symposium
              on Microarchitecture MICRO 36**
Publisher: IEEE Computer Society
Full text available: .pdf(348.55 KB)   Additional Information: full citation, abstract, index terms

In this paper we address the design of a future high-speedrouter that supports line rates as high as OC-3072 (160 Gb/s),around one hundred ports and several service classes. Buildingsuch a high-speed router would raise many technological problems,one of them being the packet buffer design, mainly becausein router design it is important to provide worst-case bandwidthguarantees and not just average-case optimizations.A previous packet buffer design provides worst-case bandwidthguarantees by using ...

10   A bit-slice cache controller
B. D. Ackland
April 1979 **Proceedings of the 6th annual symposium on Computer architecture ISCA
            '79**
Publisher: ACM Press

Full text available: .pdf(549.11 KB)   Additional Information: full citation, abstract, references, citings, index terms

Cache storage is a proven memory speedup technique in large mainframe computers. Two of the main difficulties associated with the use of this concept in small machines are the high relative cost and complexity of the cache controller. An LSI bit-slice chip set is described which should reduce both controller cost and complexity. The set will enable a memory designer to construct a wide variety of cache structures with a minimum number of components and interconnections. Design parameters ar ...

11   System-level power optimization: techniques and tools
Luca Benini, Giovanni de Micheli
April 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES),**
            Volume 5 Issue 2
Publisher: ACM Press

Full text available: .pdf(385.22 KB)   Additional Information: full citation, abstract, references, citings, index terms

This tutorial surveys design methods for energy-efficient system-level design. We consider electronic sytems consisting of a hardware platform and software layers. We consider the three major constituents of hardware that consume energy, namely computation, communication, and storage units, and we review methods of reducing their energy consumption. We also study models for analyzing the energy cost of software, and methods for energy-efficient software design and compilation. This survery ...

12   Minos: Control Data Attack Prevention Orthogonal to Memory Model
Jedidiah R. Crandall, Frederic T. Chong
December 2004 **Proceedings of the 37th annual IEEE/ACM International Symposium
              on Microarchitecture MICRO 37**

Publisher: IEEE Computer Society

Full text available: pdf(255.53 KB) Additional Information: full citation, abstract, citings

We introduce Minos, a microarchitecture that implements Biba's low-water-mark integrity policy on individual words of data. Minos stops attacks that corrupt control data to hijack program control flow but is orthogonal to the memory model. Control data is any data which is loaded into the program counter on control flow transfer, or any data used to calculate such data. The key is that Minos tracks the integrity of all data, but protects control flow by checking this integrity when a program use ...

13 Multiple operation memory structures

M. C. Ertem

August 1989 **ACM SIGMICRO Newsletter , Proceedings of the 22nd annual workshop on Microprogramming and microarchitecture MICRO 22**, Volume 20 Issue 3

Publisher: ACM Press

Full text available: pdf(693.87 KB) Additional Information: full citation, abstract, references, index terms

This paper describes architectures based on a new memory structure. Memory systems which can perform multiple transfers are described and issues in processor architecture are considered. A general model for memory operations is given, and the classical single transfer memory structures are described. Based on the generalized model, new structures which allow multiple transfers to be performed as a single processor operation are developed. Some architectural considerations at the processor I ...

14 Hive: fault containment for shared-memory multiprocessors

J. Chapin, M. Rosenblum, S. Devine, T. Lahiri, D. Teodosiu, A. Gupta

December 1995 **ACM SIGOPS Operating Systems Review , Proceedings of the fifteenth ACM symposium on Operating systems principles SOSP '95**, Volume 29 Issue 5

Publisher: ACM Press

Full text available: pdf(1.90 MB) Additional Information: full citation, references, citings, index terms

15 Cache coherence in large-scale shared-memory multiprocessors: issues and comparisons

David J. Lilja

September 1993 **ACM Computing Surveys (CSUR)**, Volume 25 Issue 3

Publisher: ACM Press

Full text available: pdf(3.12 MB) Additional Information: full citation, references, citings, index terms

16 Cryptography and data security

Dorothy Elizabeth Robling Denning

January 1982 Book

Publisher: Addison-Wesley Longman Publishing Co., Inc.

Full text available: pdf(19.47 MB) Additional Information: full citation, abstract, references, citings, index terms

From the Preface (See Front Matter for full Preface)

Electronic computers have evolved from exiguous experimental enterprises in the 1940s to prolific practical data processing systems in the 1980s. As we have come to rely on these systems to process and store data, we have also come to wonder about their ability to protect valuable data.

Data security is the science and study of methods of protecting data in computer and communication systems from unauthorized disclosure ...

17 Distributed operating systems

Andrew S. Tanenbaum, Robbert Van Renesse
December 1985 **ACM Computing Surveys (CSUR)**, Volume 17 Issue 4
Publisher: ACM Press

Full text available: 📄 pdf(5.49 MB)   Additional Information: full citation, abstract, references, citings, index terms, review

Distributed operating systems have many aspects in common with centralized ones, but they also differ in certain ways. This paper is intended as an introduction to distributed operating systems, and especially to current university research about them. After a discussion of what constitutes a distributed operating system and how it is distinguished from a computer network, various key design issues are discussed. Then several examples of current research projects are examined in some detail ...

18 The Alpha demonstration unit: a high-performance multiprocessor

Charles P. Thacker, David G. Conroy, Lawrence C. Stewart
February 1993 **Communications of the ACM**, Volume 36 Issue 2
Publisher: ACM Press

Full text available: 📄 pdf(6.26 MB)   Additional Information: full citation, references, citings, index terms, review

Keywords: Alpha AXP chip

19 Pipeline Architecture

C. V. Ramamoorthy, H. F. Li
March 1977 **ACM Computing Surveys (CSUR)**, Volume 9 Issue 1
Publisher: ACM Press
Full text available: 📄 pdf(3.53 MB)   Additional Information: full citation, references, citings, index terms

20 Virtual caches and hierarchies: Virtual private caches

Kyle J. Nesbit, James Laudon, James E. Smith
June 2007 **Proceedings of the 34th annual international symposium on Computer architecture ISCA '07**
Publisher: ACM Press
Full text available: 📄 pdf(452.49 KB)   Additional Information: full citation, abstract, references, index terms

Virtual Private Machines (VPM) provide a framework for Quality of Service (QoS) in CMP-based computer systems. VPMs incorporate microarchitecture mechanisms that allow shares of hardware resources to be allocated to executing threads, thus providing applications with an upper bound on execution time regardless of other thread activity. Virtual Private Caches (VPCs) are an important element of VPMs. VPC hardware consists of two major components: the VPC Arbiter, which manages shared cache band ...

Keywords: chip multiprocessor, performance isolation, quality of service, shared caches, soft real-time

Results 1 - 20 of 87   Result page: **1** 2 3 4 5   next

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